A Dynamically Reconfigurable Silicon Integrate-and-Fire Array Transceiver Using the Mihalas-Niebur Neuron Model

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In recent years, deep layered neural networks are habitually being used for tasks such as object recognition and classification. As intelligent systems such as autonomous drones and driver-less vehicles advance, it is essential that we perform these task faster while consuming less power. In past years, such networks have been implemented using computer programs or integrated circuits (IC), yet each implementation is flawed. Computer programs are slower than real time due to computer limitations. Also, computer software is incapable of interacting with the environment. IC's are limited in variability due to hardwired connections. Each of these methods are insufficient for deep neural networks. In order to overcome the limitations of the previous implementation methods, we propose and integrate-and-fire array transceiver (IFAT) seen in Figure 1. The IFAT does not have hardwired connections, it is reconfigurable, and it is expandable meaning multiple IFAT chips can interact with each other. Our IFAT chip is based off of a modified version of the Mihalas-Niebur neuron which is capable of reproducing nine out of the twenty observed neural behaviors. The IFAT consist of 7,752 neurons which can be used as basic leaky integrate-and-fire neurons, or two neurons can work together collectively to form one adaptive neuron utilizing the novel feature (adaptive threshold) of the Mihalas-Niebur model. We can use the IFAT for applications such as handwriting recognition, speech recognition, and object detection.

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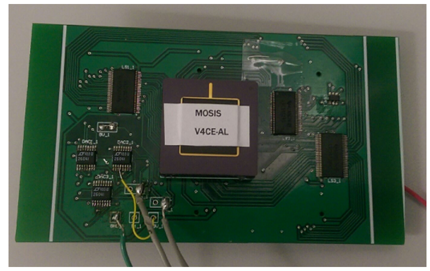

Figure 1: IFAT chip connected to PCB

We began by testing the functionality of the IFAT chip as we had received the chip from fabrication at the beginning of the summer. In order to easily interact and efficiently test the IFAT chip, we developed a graphical user interface (GUI) in Matlab seen in Figure 2.

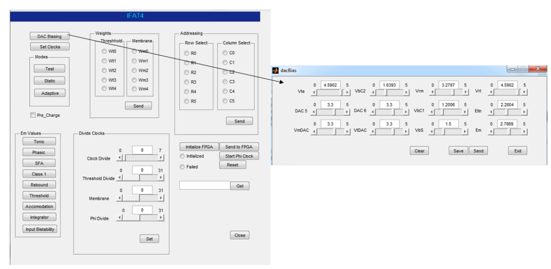

Figure 2: Graphical User Interface developed using Matlab

Using the GUI, we were able to change parameters instantly rather than waiting for the code to compile every time a change was made. During the testing phase, we noticed that the array of neurons did not operate as we had hoped. All of the neurons in the array were connected to the input of a comparator. This resulted in a charge build up at the input of the comparator which caused the membrane voltage to be at a minimum of 3 (v) instead of resetting to the reset voltage. Also, due to this charge sharing affect, the neuron would generate spikes without sending the neuron events. There could be other factors that are contributing to the problems with the chip, however we are still investigating the causes to determine a solution(s). Although the array neurons did not behave as we had hoped, we were able to demonstrate tonic spiking with the test neuron as seen in Figure 3. This is one of the nine spiking behaviors that our model is capable of. The other eight behaviors were not able to be tested within the time allotted for the project. The test neuron demonstrated proper functionality of the neuron model and it provides us with a promising hope for the future IFAT generation.

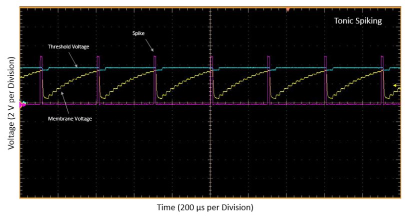

Figure 3: Tonic spiking neural behavior using the test neuron