"IEEE-1394 Motor Controller" Specification

The IEEE-1394 Motor Controller consists of a set of two boards, the IEEE-1394 FPGA Controller (IFC) board and the Quad Linear Amplifier (QLA) board. The IFC board is a general purpose IEEE-1394 FPGA board that can be used as a motor controller or for other functions. The QLA board is a 4 channel linear amplifier and interface board designed to add motor drive capability to the IFC board.

These specifications have been developed in conjunction with Johns Hopkins University Laboratory for Computational Sensing and Robotics, pursuant to deliverables for the NSF Major Research Instrumentation (MRI) grant.

IEEE-1394 FPGA Controller

The IEEE-1394 FPGA Controller Board is designed to be a general purpose FPGA board with a two port IEEE-1394 tranceiver. It will have a Xilinx Spartan®-6 XC6SLX45-2 FPGA, configuration PROM, IEEE-1394 interface, RS232 interface, connectors and required power supplies.

The board will be designed to accept the XC6SLX45, XC6SLX75, XC6SLX100 or XC6SLX150 FPGAs in the FG484 or FGG484 package. Only the LX45 FPGA will actually be installed and tested. The ability to install the larger FPGAs will not be tested and this feature is not guaranteed.

The IFC board shall have:

- A 32 megabit SPI Flash configuration PROM for the FPGA that can support MultiBoot and dynamic reprogramming.

- A two channel TSB41AB2 IEEE-1394 transceiver along with two standard 6-pin IEEE-1394 connectors.

- A 16 position rotary switch to select the IEEE-1394 node ID.

- One RS232 port with 3 transmit and 5 receive pins. The port will be available on a 10 pin header on the board.

- Ability to be powered from the IEEE-1394 bus, or from one of two power connectors on the board. The highest voltage available between the 3 sources will be used.

- Two 44 pin (2x22 pins @ 2mm pitch) connectors containing 72 general-purpose IO pins (3.3V CMOS logic level), 2 power pins and 14 ground pins.

- Ability to deliver up to 1.5A at 5.0V on the pair of power pins on the 44 pin connector.

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- Two LEDs for the status of the 5V and 3.3V power supplies, one LED indicating that the FPGA has been successfully loaded and one LED under the FPGA's control.

- The board size will be approximately 4.0" x 2.4"

The exact dimensions and connector pin-outs will be delivered with the actual boards.

Quad Linear Amplifier

The Quad Linear Amplifier board is designed to interface to the IFC board and provide the ability control up to 4 DC motors using linear current control. Connectors and mounting holes will be located to allow the smaller IFC board to be mounted on top of the larger QLA board.

The QLA board consists of Digital to Analog Converters (DACs) writeable by the FPGA to specify the motor current driven by the linear amplifiers and Analog to Digital Converters (ADCs), readable by the FPGA to allow monitoring the motor current. Digital and analog feedback from the robot is present in the I/O connector and is made available to the FPGA to allow closed loop control.

The actual circuit for the Linear Amplifiers, the number and type of I/O signals, the I/O connector and its pin-out has been specified by the Johns Hopkins University Laboratory for Computational Sensing and Robotics (JHU LCSR).

The amplifier section of the QLA board shall have:

- Four identical analog power amplifiers, each amplifier consisting of two OPA549 op-amps implementing the "Precision Current Control" circuit specified by JHU LCSR.

- Each channel shall be capable of up to $\pm$7.5A at up to 48V, limited to 15A per board. The actual drive capability may be lower, depending upon the heatsink design, the heatsink's ability to dissipate power and the maximum current of the actual power supply.

- Each channel's drive current shall be specified by an independent 16 bit DAC ($\pm$15 bits range), capable of being written by the FPGA.

- Each channel's actual current shall be monitored by an independent 16 bit ADC ($\pm$15 bits range), capable of being read by the FPGA at a rate of 100K samples per second or higher.

- Each channel's drive signals shall be brought to a female DB-9 connector. The pin-out of the connector will be documented with the delivered hardware.

- Each channel shall have an independent enable signal, controllable by the FPGA.

- Each channel shall have a status signal that shall be available to the FPGA as well as used to drive a status LED. The LED shall be green when the channel is active and off when the channel is disabled or in fault.

- A dedicated 4 pin power connector will provide 12V to 48V at up to 15A for the power amplifiers. A comparator will monitor this voltage and set a flag when the voltage on this connector is within the specified limits. The flag will be available to the FPGA and used to drive a status LED. The LED will be green when the voltage is within specifications.

- There will be two temperature sensors, located to measure the temperature of the heat sink at two locations. These will be temperature to frequency converters with the frequency outputs available to the FPGA.

The QLA board shall have an I/O connector. The connector type and pin-out will be as specified by JHU LCSR and will be documented with the delivered hardware. The I/O connector will have:

- 12 un-terminated differential inputs. These inputs will be converted to 3.3V CMOS logic level and be available to the FPGA. While intended for use by incremental encoders, they can be assigned any functions supported by the FPGA.

- 12 single ended inputs, individually pulled up to 5V through 2.7K resistors. These inputs will be converted to 3.3V CMOS logic level using a 2.5V threshold and be available to the FPGA. While intended for use by limit and home switches, they can be assigned any functions supported by the FPGA.

- 5V power output, divided into two groups, each group current limited to a minimum of 250mA. This is intended to power incremental encoders and active limit switches.

- 4 analog inputs and corresponding 4.5V reference voltage, current limited to 100mA. Each analog input is filtered at 60Hz and resolved between ground and the provided reference voltage using an independent 16 bit ADC, capable of being read by the FPGA at a rate of 100K samples per second or higher.

- 4 digital outputs, independently controlled by the FPGA. Each output is switched to ground using an "Intellifet" MOSFET. The Intellifet is current limited to 1A (minimum) and provides over-current and over-temperature shutdown.

The QLA board shall have the following additional features:

- Two 3-pin "safety loop" connectors. The connection between pin 2 to pin 2 will always be present. The connection between pin 1 to pin 1 and pin 3 to pin 3 will be normally open and can be closed using a relay under the FPGA's control.

- Two bi-color status LEDs controllable by the FPGA. This will be in addition to 4 green status LEDs for the 4 amplifiers, green status LEDs for the amplifier power and a green status LED for the 5V power.

- Everything on the board described up to this point, except the OPA549s, will operate from the 5V provided by the FPGA board, or other voltages derived from the 5V.

- A DC-DC converter will generate 12V at 2A (or 2V below input voltage when input voltage is below 14V) from the amplifier input voltage. This voltage will be available on three 2-pin connectors. This is intended to be used by heat sink fans and optionally to power the FPGA board when a safety loop is not in use.